We claim:

1. A pulse shaping system comprising:

a first parallel-to-serial converting unit capable of being triggered for operation by a leading edge or a trailing edge of a predetermined clock signal to convert first parallel data into an initial serial data pulse;

a second parallel-to-serial converting unit capable of being triggered for operation by the trailing edge of the clock signal if the first parallel-to-serial converting unit is triggered by the leading edge of the clock signal or by the leading edge of the clock signal if the first parallel-to-serial converting unit is triggered by the trailing edge of the clock signal to convert second parallel data into a pulse width adjusting serial data pulse;

a pulse width adjusting unit for adjusting width of the initial serial data pulse between at least one of edges of the initial serial data pulse and an edge of the pulse width adjusting serial data pulse; and

a serial data output unit that provides a serial data pulse of a pulse width adjusted by the pulse width adjusting unit.

2. A pulse shaping system comprising:

a clock signal delaying unit including a plurality of signal delay devices placed in a predetermined clock signal line to obtain delayed pulses at a plurality of delayed times

by delaying leading and trailing edges of a clock signal; and

a delayed pulse gate that passes the delayed pulse of a time specified by a timing signal specifying the time of the delayed pulse.

3. The pulse shaping system according to claim 2, wherein at least one circuit of the same configuration as the clock signal delaying unit and the delayed pulse gate is formed as an nth-stage delay circuit (n is a natural number not smaller than 2), a delayed pulse passed the (n-1)th-stage delayed pulse gate is applied to a clock signal line of the nth-stage delay circuit.

4. A pulse shaping system comprising:

a first parallel-to-serial converting unit capable of being triggered for operation by the leading edge or the trailing edge of a predetermined clock signal to convert first parallel data into an initial serial data pulse;

a second parallel-to-serial converting unit capable of being triggered for operation by the trailing edge of the clock signal if the first parallel-to-serial converting unit is triggered by the leading edge of the clock signal or by the leading edge of the clock signal if the first parallel-to-serial converting unit is triggered by the trailing edge of the clock signal to convert second parallel data into a pulse width adjusting serial data pulse;

a pulse width adjusting unit for adjusting the width of

the initial serial data pulse between at least one of the edges of the initial serial data pulse and the edge of the pulse width adjusting serial data pulse;

a serial data output unit that provides a serial data pulse of a pulse width adjusted by the pulse width adjusting unit;

an n-stage clock signal delaying unit (n is a natural number) including a plurality of signal delay devices placed in a predetermined clock signal line to obtain delayed pulses at a plurality of delayed times by delaying a leading and a trailing edge of a clock signal;

an n-stage delayed pulse gate (n is a natural number) that passes the delayed pulse of a time specified by a timing signal specifying the time of the delayed pulse;

a delayed pulse input unit for applying the delayed pulse passed the nth delayed pulse gate to a clock signal line of an (n+1)th clock signal delaying unit;

a delayed clock selecting unit for selecting a delayed pulse according to a delayed clock selection signal specifying one of the n-stages of delayed pulse gates; and

a high-resolution serial data pulse signal output unit for providing a high-resolution serial data pulse formed by adjusting the pulse width of the serial data pulse between at least one of the edges of a serial data pulse provided by the serial data output unit and the edge of the delayed pulse

selected by the delay clock selecting unit.

5. The pulse shaping system according to claim 4, wherein the high-resolution serial data pulse is used for adjusting width of a laser beam in a scanning direction of a laser printer.

6. The pulse shaping system according to claim 1 or 4, wherein the second parallel-to-serial converting unit includes a shift register driven by either the leading or the trailing edge, and a flip-flop capable of latching an output of the shift register and driven by the leading edge when the shift register is driven by the trailing edge or by the trailing edge when the shift register is driven by the leading edge.

7. The pulse shaping system according to claim 1, wherein the pulse width is adjusted by either the pulse width adjusting unit or the high-resolution serial data pulse signal output unit, or by a combination of the pulse width adjusting unit and the high-resolution serial data pulse signal output unit, and an edge of the pulse to be subjected to width adjustment and an edge of a pulse to be compared correspond to different times, respectively.

8. The pulse shaping system according to claim 2, wherein the signal delay device is a buffer provided with an even number of inverters.

9. The pulse shaping system according to claim 2, wherein the timing signal is a parallel output signal provided

by a register that specifies a delayed pulse by setting each of bits to the ON state or the OFF state.

10. The pulse shaping system according to claim 2, wherein the number of the plurality of signal delay devices is determined such that a time interval between the most delayed signal among those delayed by the plurality of signal delay devices, and a nondelayed signal is 3/2 of a necessary delay time of the delayed pulse or below.

11. A laser printer that performs a printing operation by controlling a laser beam emitted by a printer engine on the basis of serial video data specifying width of the laser beam with respect to a scanning direction corresponding to tones of dots, said laser printer comprising:

a first parallel-to-serial converting unit capable of being triggered for operation by the leading edge or the trailing edge of a predetermined clock signal to convert first parallel data into an initial serial data pulse of a resolution lower than a resolution needed by the serial video data and having pulse width that changes in a unit length corresponding to a period of the clock signal;

a second parallel-to-serial converting unit capable of being triggered for operation by the trailing edge of the clock signal if the first parallel-to-serial converting unit is triggered by the leading edge of the clock signal or by the leading edge of the clock signal if the first parallel-to-

serial converting unit is triggered by the trailing edge of the clock signal to convert second parallel data into a pulse width adjusting serial data pulse having pulse width that changes in a unit length corresponding to the period of the clock signal;

a pulse width adjusting unit for adjusting width of the initial serial data pulse between at least one of the edges of the initial serial data pulse and an edge of the pulse width adjusting serial data pulse;

a serial data output unit that provides a pulse of a pulse width adjusted by the pulse width adjusting unit or the initial serial data pulse as a serial data pulse;

an n-stage clock signal delaying unit (n is a natural number) including a plurality of signal delay devices placed in a predetermined clock signal line to obtain delayed pulses at a plurality of delayed times by delaying a leading and a trailing edge of a clock signal;

an n-stage delayed pulse gate (n is a natural number) that passes a delayed pulse of time specified by a timing signal specifying the time of the delayed pulse;

a delayed pulse input unit for applying the delayed pulse passed the nth delayed pulse gate to a clock signal line of an (n+1)th clock signal delaying unit;

a delayed clock selecting unit for selecting a delayed pulse according to a delayed clock selection signal specifying

one of the n-stages of delayed pulse gates to increase pulse width of the serial data pulse in a unit corresponding to 1/N (N = n + 1) of half the period of the clock signal; and

a high-resolution serial data pulse signal output unit for providing a high-resolution serial data pulse formed by adjusting the pulse width of the serial data pulse between at least one of the edges of a serial data pulse provided by the serial data output unit and the edge of the delayed pulse selected by the delay clock selecting unit.

12. A pulse shaping method comprising the steps of:

converting a first parallel data into an initial serial data pulse by a circuit capable of being triggered for operation by a leading edge or a trailing edge of a predetermined clock signal;

converting second parallel data into a pulse width adjusting serial data pulse by a second parallel-to-serial converting unit capable of being triggered for operation by the trailing edge of the clock signal if the first parallel-to-serial converting unit is triggered by the leading edge of the clock signal or by the leading edge of the clock signal if the first parallel-to-serial converting unit is triggered by the trailing edge of the clock signal; and

adjusting width of the initial serial data pulse between at least one of edges of the initial serial data pulse and an edge of the pulse width adjusting serial data pulse and

providing a pulse of an adjusted pulse width as a serial data pulse.

13. A pulse shaping method comprising the steps of:

providing delayed pulses at a plurality of delayed times by delaying leading and trailing edges of a clock signal by a clock signal delaying unit including a plurality of signal delay devices; and

giving a timing signal specifying one of delayed pulses at the plurality of times to a predetermined delayed pulse gate to pass the delayed pulse of a time specified by the timing signal.

14. A pulse shaping method comprising the steps of:

converting first parallel data into an initial serial data pulse by a first circuit capable of being triggered for operation by a leading edge or a trailing edge of a predetermined clock signal;

converting second parallel data into a pulse width adjusting serial data pulse by a second circuit capable of being triggered for operation by the trailing edge of the clock signal if the first circuit is triggered by the leading edge of the clock signal or by the leading edge of the clock signal if the first circuit is triggered by the trailing edge of the clock signal;

adjusting width of the initial serial data pulse between at least one of the edges of the initial serial data pulse and

an edge of the pulse width adjusting serial data pulse to provide the pulse of the adjusted width as a serial data pulse;

selectively providing a delayed pulse according to a delayed clock selecting signal specifying one of n delayed pulse gates by repeating n times the steps of generating delayed pulses at a plurality of delayed times by delaying leading and trailing edges of a clock signal by a clock signal delaying unit including a plurality of signal delay devices, giving a timing signal specifying one of delayed pulses to a predetermined delayed pulse gate to pass the specified delayed pulse and giving the delayed pulse to a following delayed pulse gate; and

providing a serial data pulse of a pulse width adjusted between at least one of edges of the serial data pulse and an edge of the selected delayed pulse as a high-resolution serial data pulse.

15. A serial video data generating method to be carried out by a laser printer that performs a printing operation by controlling a laser beam emitted by a printer engine on the basis of serial video data specifying width of the laser beam with respect to a scanning direction corresponding to tones of dots, said serial video data generating method comprising the steps of:

converting first parallel data into an initial serial data pulse of a resolution lower than a resolution needed by

the serial video data and having pulse width that changes in a unit length corresponding to a period of the clock signal by a first circuit capable of being triggered for operation by a leading edge or a trailing edge of a predetermined clock signal;

converting second parallel data into a pulse width adjusting serial data pulse having pulse width that changes in a unit length corresponding to the period of the clock signal by a second circuit capable of being triggered for operation by the trailing edge of the clock signal if the first circuit is triggered by the leading edge of the clock signal or by the leading edge of the clock signal if the first circuit is triggered by the trailing edge of the clock signal;

adjusting width of the initial serial data pulse between at least one of edges of the initial serial data pulse and an edge of the pulse width adjusting serial data pulse;

providing a pulse of a pulse width adjusted by pulse width adjustment or the initial serial data pulse as a serial data pulse;

selectively providing a delayed pulse according to a delayed clock selecting signal specifying one of n delayed pulse gates by repeating n times (n is a natural number) the steps of generating delayed pulses at a plurality of delayed times by delaying leading and trailing edges of a clock signal by a clock signal delaying unit including a plurality of signal

delay devices, giving a timing signal specifying one of delayed pulses to a predetermined delayed pulse gate to pass the specified delayed pulse and giving the delayed pulse to a following delayed pulse gate, and selectively providing a delayed pulse according to a delayed clock selection signal specifying one of the n-stages of delayed pulse gates to increase pulse width of the serial data pulse in a unit corresponding to 1/N (N = n + 1) of half the period of the clock signal; and

adjusting width of the serial data pulse between at least one of edges of the serial data pulse and an edge of the selectively provided delayed pulse to give the serial data pulse having the adjusted pulse width as a high-resolution serial video data to the printer engine.